Article from the April 2001 issue of Electronic Journal

Intel's 300mm Program is On-Line

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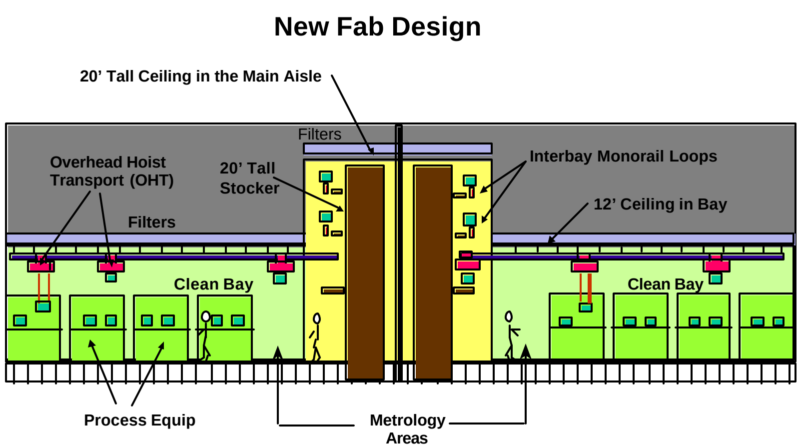
Enter into D1C, Intel's new 300mm Technology Development facility, and the difference from a 200mm factory is immediately apparent. Look up in the main aisle and one views a 3 level automation system with stockers that seem as tall as skyscrapers all interconnected by monorails and linked with every tool (production equipment) in the factory via an overhead vehicle transport system (OHV). This factory was designed with full factory automation in mind. Looking around the fab, it is clear that the tools are of a new breed. Every tool has a mini-environment to isolate wafers from the open fab air. The tools are much larger in both footprint and height. Some tools, like wet benches and implanters, are big enough to walk inside for servicing. It is very clear that something big has happened and semiconductor factories have finally found the compelling reason to fully automate operations.

Figure 1. Multilevel AMHS



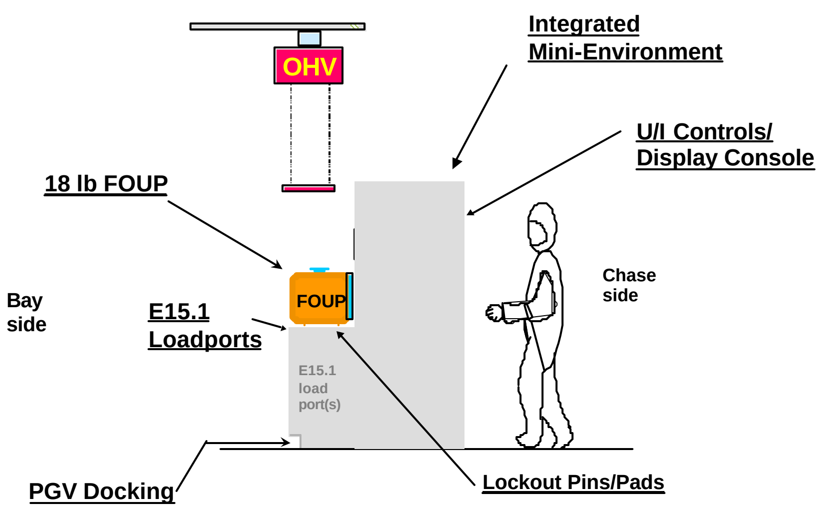
The Mechanized Factory

The conversion to 300mm wafers compels a change to fully automated material transport throughout the factory. The weight of a 25 wafer run box, now called a FOUP (Front Opening Unified Pod) is 18 pounds. The FOUP is too heavy to be carried around the factory and handled manually, by people, on a repeated basis. Additionally, the use of manual carts in high volume manufacturing will not work efficiently. The carts, called PGV's (Personnel Guided Vehicles), can carry only two FOUP's at a time and would require significant space for maneuvering and parking in the valuable cleanroom space.

When D1C was designed, material storage space became a key concern due to the large size of the FOUP. FOUP volume is 325% larger than a 200mm box. It was estimated that stocker floor space would nearly double and consume an additional 3-5% of the total factory floor space. The space problem drove a decision to go vertical and use stockers that are over 20 feet tall. The stockers are all aligned and concentrated along the center of the factory and interconnected via 2 levels of interbay monorail to speed up material transport and save space. The stockers are connected at a third level which are the intrabay transport loops on which the Overhead Hoist Vehicles (OHV) operate and deliver FOUPs to production equipment in each bay. This multi-level interconnect system works much like chip design in that as the need for more interconnect points (tools) goes up it becomes necessary to add additional layers, otherwise the system will be too slow or the factory layout would have to spread out to allow for more parallel paths and crossover points. Looking up in this factory you will view the world's first semiconductor multi-level automation system!

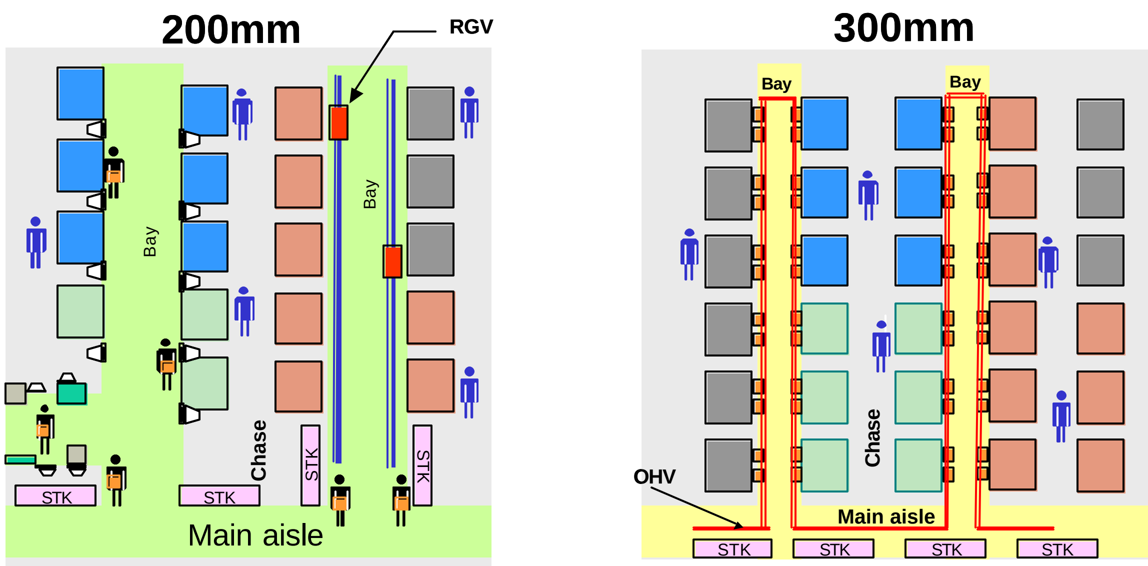
Another significant difference that can be seen in D1C is that all tools are designed with mini-environments and common load-port interfaces to facilitate FOUP loading and unloading by OHV system. Because wafers are isolated from the open fab environment by the FOUP and mini-environment, a slightly lower class of cleanroom is allowed in the bays and technicians no longer have to wear the special helmets with portable filters (which are common in 200mm) and can instead wear hoods. The excellent collaborative work on standards by the IC makers and equipment suppliers has finally paid off.

Figure 2. Mini-Environment and OHV



With the advent of the OHV system for movement of wafers between stockers and tools, the lots not only move faster but also enable the use of narrower bays. Because floor running rail-guided intrabay vehicles no longer run down the bay at floor level (common in 200mm), the extra clearance space is not needed and significant floor space can be saved. In high volume manufacturing, technicians will operate the tools from either the chase rear of the tool or remote command centers and will call for lots to be delivered to the tools. So, much like a chip, narrower lines (bays) allow more tools to be put into an equivalent space.

Fig. 3
High Volume Manufacturing Layout Differences



- **Manual wip movement and RGV**
- **Wider bays for Operators**
- **Wip racks, workstations in bays**

- **100% OHV automated material handling**
- **Narrow bays; Operators in the chase.**
- **Command centers for wip movement.**

With mechanization of the total factory and the use of the overhead hoist transport system, precise placement of tools has become critical. The tool load ports must be aligned with the centerline of the OHV track to within a few millimeters. This means that detailed alignment procedures must be in place when installing the tools. Any error in placement of the tool means costly repositioning and delays. The D1C factory displays a unique combination of multi-level automation and narrow bays combined with high-precision tool placement.

Figure 5.
Multilevel AMHS

Figure 4.
OHV and a FOUP

Intel's 300mm manufacturing factories will be fully automated. Factories will have a completely automated material handling system with integrated material scheduling and movement. There will also be a web-enabled decision support system along with extensive use of remote e-diagnostic capability.

0.13um on 300mm Wafers

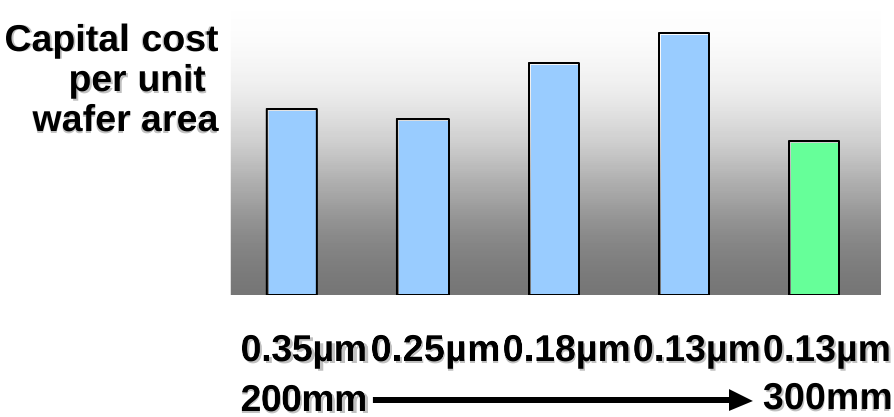
Intel's D1C, the world's first 300mm 0.13um factory, is now in full development. This is the same industry-leading 0.13 um technology with 0.07um gate lengths that was described in the press release in November 2000 and at the International Electron Devices meeting in December 2000. The circuit is an 18MB SRAM incorporating more than 100M transistors that operates at >1.6GHz. Pilot line operations started in the 4th quarter of 2000. The first wave of development tools are installed and fully operational; a second group targeted for 0.10um development is in the process of being installed. The startup approach has been to test and match modules with the 200mm 0.13um baseline process. This is consistent with our "copy exactly" policy and represents the lowest risk approach. This matching approach will continue throughout the development phase. The 0.13um production ramp is expected to start in 2002. The second 300mm factory, Fab 11X in New Mexico, follows D1C into production by about 2 quarters. These 300mm factories will greatly increase Intel's CPU output while reducing costs and environmental impact. Regardless of the various industry scenarios, it will take several factories to meet the demands for 0.13um output. If Intel were only planning on 200mm capacity, even more factories would be needed.

Moore's Law + 300mm Wafers = 4X Advantage
Conversion to 300mm at the 0.13um generation makes it ~4X more productive than the previous 0.18um generation. Following Moore's Law, the density improvement between 0.18um and 0.13um gives the equivalent of a 2X improvement in output. The conversion to 300mm wafers provides an additional 2X improvement in output. The combined output advantage is equal to 4X per wafer.

300mm- Lowers Production Cost
Intel's conversion to 300mm is driven entirely by cost. A 30% cost reduction is expected on wafers of the same technology generation. With improved productivity and an expected cost reduction, the conversion to 300mm becomes even more compelling when combined with the fact that all new technology development will be done on 300mm wafers. The next generation process tools are all being developed on 300mm platforms. At the 0.13um generation, about 30% of the 200mm tools are on 300mm platforms, and that will increase with each new generation. Any company that does not convert to 300mm wafers will be at an increasing disadvantage because 300mm tools running 200mm wafers (bridge tools) are not as productive (larger footprint, same or less wafer output). While tool footprints increased, the average tool output improved to the extent that a 300mm factory can produce 1.6-2.0X the amount of chips that an equivalent sized 200mm factory can produce.

The previous 200mm wafer size conversion only enabled a 1.2X improvement in output. The die scalar of a 300mm wafer compared to a 200mm wafer is 2.25-2.5 depending on die-size. The die scalar for 200mm wafers compared to 150mm wafers was only about 1.9. This difference in scalars from the previous wafer size conversion enables an improved, if not compelling, opportunity for cost reduction.

Figure6. 300mm Rolls Cost Back



Reduced Environmental Impact

300mm factories will be the most environmentally effective in the company. Early in the 300mm equipment product development cycle, rigorous industry expectations were defined with regard to resource consumption and environmental emissions limits. The tool suppliers have made considerable progress in these areas. On a given technology, 40-50% fewer factories are required for 300mm to produce the same amount of die as compared to 200mm. Power and water consumption per die are reduced by ~40%. Air emissions are reduced by 35-40%. In a world increasingly concerned about consumption of natural resources and environmental emissions, this is welcome news.

With the reduction in the number of factories needed for a given technology generation, the productivity of factory workers almost doubles with the use of 300mm wafers.

The Equipment

The new tools for 300mm appear to be based on better designs than any previous wafer-size generation. The equipment manufacturers paid attention to the many problems that were found on the older 200mm tools and designed them out. Only time will tell as to how well the tools perform. The concern now is that the suppliers must get the infrastructure in place to support the new tools as they proliferate.

This totally new equipment set has provided a new set of challenges for engineers and technicians. All new tools introduce new problems into a factory. Interoperability issues between FOUP's, the hundreds of equipment loadports, and the OHV system must be resolved quickly and proactively. Factories must be able to use multiple FOUP manufacturers simultaneously without tool adjustment. Additionally, the quality and design of the FOUPS must improve, as there are still issues to be resolved. The new mini-environments and robots add new failure modes in the tools. Larger chambers, platens, and furnaces provide new opportunities for process shifts and uniformity changes that need to be characterized and optimized. Tool suppliers are stressed to retrain their complete service engineer base on the new tools and to work through the myriad of new equipment problems.

One of the most important areas for attention by the tool manufacturers is the spare parts system. New tool designs result in many new failure mechanisms and a solid spare parts supply line is crucial to quick resolution of problems. Intel recognized that spare parts supply was an important factor in a successful wafer size conversion and started work on the problem long before tools were delivered. Many of the tool suppliers have put solid systems in place for field service personnel and spare parts, however, there are still some who are in need of improvement.

Summary

A 300mm factory is very different from the traditional semiconductor factory. The tools are all new, they are larger, full mechanization has become a necessity, and the mini-environment is now a standard. Intel's 300mm production factories will be fully automated in manufacturing including integrated and synchronized material scheduling and movement.

D1C, the first 300mm 0.13um factory, has started process development. Intel's decision to convert to 300mm wafers was driven by cost, and conversion at the 0.13um generation provides

a 4X gain in productivity (vs 200mm, 0.18um current generation). Other companies have demonstrated 300mm wafers at the 0.25um and 0.18um generations.
Production output on the 0.13um technology for 300mm will be in 2002. Product produced on both 200mm and 300mm 0.13um process wafers will have the same electrical characteristics.

All future process technologies, 0.10um and beyond, will be developed on 300mm wafers. The driving reason for this is that the next generation tools are being developed on 300mm platforms, which will translate into a disadvantage for those who do not convert to 300mm wafers.

Acknowledgements
I would like to recognize the work of the team making the 300mm conversion happen at Intel. In addition I would like to recognize the support of Mung Chen, Paolo Gargini, Jerry Marcyk, Mark Bohr, Dave Krick, Dev Pillai, and Howard High.

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All references may be found on Intel's Silicon Showcase at
http://www.intel.com/research/silicon/

Biography: Tom Garrett is the D1C and 300mm Program Manager in the Logic Technology Development group at Intel in Oregon. Tom has been at Intel for over 24 years, working in various Fab management positions and has been in the Technology Development organization since 1987. Tom was the startup manager for the 0.18um development factory, D1B, in Oregon. In late 1996 he started managing the D1C and the 300mm programs. Tom graduated with a BS degree from California State University, Fresno, in 1973. He first worked at Applied Materials for 3 years before coming to Intel in 1976. Tom's interests outside of family, which includes his wife and 3 daughters, and work, are fly fishing, sailing, and raising horses. His email address is Thomas.Garrett@intel.com.